By the present amendment, the original claims 1-16 have been cancelled without prejudice and replaced by new claims 17-35. It is noted that new claims 19, 22 and 26 correspond, respectively, to claims 3, 6 and 10 rewritten into independent form to include all limitations from their parent claims, together with appropriate amendments to overcome the objections and 35 U.S.C. 112 rejection set forth in the Office Action. Accordingly, entry and allowance of new claims 16, 22 and 26 is respectfully requested based upon the indication of allowable subject matter in the Office Action.

Also by the present amendment, the rejected claims 1, 2, 4, 5, 7-9 and 13-16 have been replaced by new claims 17, 18, 20, 21, 23-25 and 27-30, respectively. In each case, claims have been amended to clarify the invention and to overcome the objections and 35 U.S.C. 112, second paragraph, rejection set forth in the Office Action. Based on these amendments, reconsideration and removal of the objection to the claims and the 35 U.S.C. 112, second paragraph, rejection set forth in the Office Action is respectfully requested. Allowance of these claims over the prior art rejection based on Mizuno is also respectfully requested for reasons set forth below.

In addition, the title has been revised and minor corrections of informalities in the specification, including those set forth in paragraph 2 of the Office Action, have been made. Accordingly, reconsideration and removal of the objection to the title and the specification set forth in paragraphs 1 and 2 of the Office Action is respectfully requested.

Finally, the present amendment adds new means-plus-function claims 31-35 to define the invention from a different perspective. It is respectfully submitted that these claims clearly define over the cited prior art, for reasons which will be discussed below.

Reconsideration and removal of the objection to Fig. 3 as needing to be labeled as prior art is respectfully requested. Basically, although Fig. 3 does show characteristic curves of the best to the worst characteristics that can pertain to prior art devices, it also describes how the present invention can be operated based on typical values rather than a worse case value. This description pertains to the labeling (A, B, C) (A', B', C') and (A", B", C") shown in Fig. 3. The significance of these labeled portions of the drawing with regard to the present invention is discussed on page 11, line 15 through page 12, line 4. By virtue of this labeling and description concerning the present invention, it is respectfully submitted that Fig. 3 actually represents an aspect of the present invention, and, as such, should not be labeled as prior art since this would mislead one to believe that the analysis of these labeled regions had been previously done. Accordingly, reconsideration and removal of this objection is respectfully requested.

Turning to the merits of the case, briefly, the present invention is directed to a problem which the inventors have determined that, for CMOS transistors as the operating speed is increased, the power consumption also increases. This serves to increase the heat in the device and deteriorate operation, as discussed on page 1, line 7 et seq. The present invention is directed to permitting CMOS transistors to operate at high speed with lower overall power by permitting the setting of characteristics for a typical case shown in Fig. 3 rather than a worse case situation, which has been done in the past.

Referring to Fig. 3, this figure shows fluctuation of characteristics in production processing for forming CMOS devices. In particular, Fig. 3 shows that, even with the same supply voltage, one can have different operating frequencies depending on whether the device is best, typical or worst. In the prior art, as

discussed beginning on page 3, line 12 et seq., systems were designed for the worst case. Therefore, a voltage Vdd equal to 1.2 volts would be set to ensure 100 mhz operation.

The objection of the present invention is to suppress characteristic variations of the CMOS devices (e.g., see page 4, line 10 et seq.) and to permit operation at low power and high speed. Basically, the inventors want to be able to guarantee at least typical case operation for design rather than having to design for the worse case situation shown in Fig. 3.

In their studies, the inventors determined that this goal can be achieved if one controls all three elements of the operating frequency of the clock signal, the supply voltage Vdd and the substrate bias voltage Vbb, as discussed on page 4, line 3 et seq. In particular, as noted on page 11, line 26 et seq.:

> "By controlling the substrate bias, the operating clock frequency and the supply voltage as mentioned above, the control point A, B or C of the main circuit LSI may be shifted to the control point A', B' or C' for lowering the power consumption or the control point A", B", or C" for enhancing the operating speed."

Fig. 1 provides an illustration of an embodiment of the present invention for carrying out this control of all three characteristics of clock voltage frequency, supply voltage and substrate bias voltage. Fig. 6 shows a flow chart for one embodiment utilizing the structure of Fig. 1. As shown in Figs. 1 and 6, the clock frequency is controlled by the clock frequency control circuit FRQCNT in response to a command signal CMDO1 provided by the command generating circuit OP. The power supply voltage is controlled by power supply voltage control circuit VDDCNT in response to a command CMDO2, while the substrate bias voltage is controlled by the substrate bias controller VBBCNT in response to a command signal CMDO3 from the

command generating circuit OP. As such, the three characteristics of the CMOS logic circuit LOG and th main circuit LSI are controlled.

Referring to the embodiment of Fig. 6, one way to achieve this is to set the clock frequency first, followed by looking up initial values of VDD and VBB for the set clock frequency in the table, TBL (e.g., see page 16, line 23 et seq.)

Next, the power supply voltage VDD is adjusted with the control circuit VDDCNT. Then, as noted on page 17, line 4 et seq.:

> "Lastly, the substrate bias controlling circuit VBBCNT selects the optimum substrate bias so that the main circuit meets the requested performance, based on the block signal and the supply voltage. When the optimum substrate bias is selected, the main circuit starts its operation."

Fig. 14 shows one example of a monitoring circuit which can carry out the performance monitoring shown in Fig. 6.

The advantage of the arrangement of the Fig. 6 embodiment is noted on page 17, line 13 et seq. as:

> "Then, the substrate bias is being adjusted as feeding back the data as to whether the operation of the main circuit may meet the requested performance. This adjustment results in realizing the operation at the lowest possible power consumption as meeting the requested performance."

Other similar embodiments which have similar advantages are shown in Figs. 7-13.

Reconsideration and allowance of newly submitted claims 17, 18, 20, 21, 23-25 and 27-30 (corresponding to claims 1, 2, 4, 5, 7-9 and 13-16, respectively) over Mizuno is respectfully requested.

By the present amendment, each of the independent claims 17, 25 and 27 has been amended to particularly define the feature of the present invention of:

> " wherein the frequency of the clock signal, the supply voltage and the substrate bias voltage are adjusted according to an operating performance of the first circuit"

It is respectfully submitted that Mizuno fails to teach or suggest any such arrangement of initial values of all three characteristics of th frequency of the clock signal, the supply voltage and the substrate bias voltage based on predetermined combinations.

Referring to Mizuno, column 6, line 66 through column 7, line 5 states:

> "Generally, when a high oscillation frequency is selected for the high-speed operation by setting a lower threshold voltage, the power consumption increases due to the sub-threshold leakage current, whereas when a lower oscillation frequency is selected by setting a higher threshold voltage, the power consumption decreases in exchange for a lower operation speed."

Thus, when high speed operation is not necessary, the operating frequency in Mizuno is low. Mizuno increases the threshold voltage of the transistors so that power consumption caused by the sub-threshold leakage current will decrease without adversely affecting the operating speed. On the other hand, when high-speed operation is required, Mizuno decreases the threshold voltage to obtain the necessary operating speed.

As noted in the Office Action, Mizuno is concerned with controlling threshold voltage, not supply voltage. Of course, as noted on page 2, lines 10-23 of the specification of the present application, it has been known in the past to control supply voltage. However, there is no suggestion in Mizuno as to how one would incorporate of supply voltage in conjunction with controlling threshold voltage and operating speed. In fact, there are infinite possible combinations and infinite unsuitable combinations of these elements. Although Mizuno includes a monitoring circuit, finding a suitable combination of threshold voltage and supply voltage would require a very large amount of time. Beyond this, Mizuno makes no suggestion of using the monitoring circuit to find appropriate values regarding threshold voltage,

amp rejection was made under 103

Ant ??

So what?

amp - no it wouldn't

supply voltage and clock frequency. As noted above, each of the independent claims 17, 25 and 27 provides <u>initial values</u> for the clock frequency, the supply voltage and the substrate bias voltage "based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage." This permits setting the characteristics for the most preferable condition (at least the typical case in Fig. 3) as discussed on page 11, line 15 through page 12, line 2 as well as on page 20, lines 1-6. Examples for setting the initial values based on predetermined combinations are described in the various embodiments of Figs. 6-13. In every instance, tables of predetermined combinations TBL are provided. Mizuno is completely devoid of any such teaching. Accordingly, reconsideration and allowance of new claims 17, 18, 20, 21, 23-25 and 27-30 over Mizuno is earnestly solicited.

So what? - it's routine [illegible]

Reconsideration and allowance of newly submitted claims 31-35 over Mizuno is also respectfully requested. New claim 31 is similar to claim 17, but defines the invention specifically in means-plus-function format. As such, claim 31 defines means for adjusting the frequency of the clock signal, the supply voltage and the substrate bias voltage according to the operating performance of the first circuit. In addition, it further defines means for deciding initial values of the frequency of the clock signal, the supply voltage and the substrate bias voltage based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage. Again, nothing in Mizuno suggests any such structure or operation.

No

New independent claim 33 particularly defines the steps shown in Fig. 6 in means-plus-function format. As such, the claim defines means for setting the clock frequency in accordance with the first command, means for setting initial values of

th supply voltage and substrate bias voltage based on the set clock frequency and means for adjusting the supply voltage, and the substrate bias voltage based on the set initial values. In addition, the claim defines means for evaluating performance of the first circuit based on the set values of the clock frequency supply voltage and substrate bias voltage, <u>and means for adjusting the initial value of the substrate bias voltage based on the evaluated performance of the first circuit</u>. It is respectfully submitted that nothing in Mizuno teaches or suggests this combination of features in this operation.

Accordingly, reconsideration and allowance of new independent claims 31 and 33 is also respectfully requested.

Dependent claim 32 corresponds to dependent claim 18, and further defines the command generating circuit operation. New dependent claims 34 and 35 specifically define the use of a correspondence table such as shown in Figs. 6 – 13 for the setting of initial values. Again, Mizuno is devoid of such an arrangement. Therefore, reconsideration and allowance of the dependent claims 32, 34 and 35 over Mizuno is also respectfully requested.

Attached hereto is a marked-up version of the changes made to the title, specification and claims by the current amendment. The attached page is captioned "<u>Version with markings to show changes made.</u>"

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the

filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (500.39910X00).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By

Gregory E. Montone
Registration No. 28,141

GEM/kd
703/312-6600

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Title:

The title has been amended as follows:

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE IN WHICH OPERATING FREQUENCY, SUPPLY VOLTAGE AND SUBSTRATE BIAS VOLTAGE ARE CONTROLLABLE TO REDUCE POWER CONSUMPTION

In the Specification:

Page 1, paragraph beginning at line 2, has been amended as indicated below:

The present invention relates to a semiconductor integrated circuit device, and more particularly to [the] a semiconductor integrated circuit device which may be operated at both high speed and low electric power.

Page 1, paragraph beginning at line 7 and continuing through page 2, has been amended as indicated below:

In order to improve the performance of [the] semiconductor integrated circuit [device] devices composed of [a] CMOS [circuit] circuits, some methods have been proposed such as shrinkage of [a] MOS [transistor] transistors that [is] are a [component] components of the CMOS [circuit] circuitry, lowering of [an] absolute [value] values of [a] threshold [voltage] voltages of the MOS [transistor] transistors, and raising of a supply voltage. In [actual] actuality, however, with improvement of an operating speed of the CMOS circuit, the power consumption is increased accordingly. For example, as the threshold voltage of the MOS transistor is made

lower and lower, the operating speed becomes higher and higher, [though] but the leak current is also increased [more]. Likewise, with enhancement of the supply voltage, the operating speed is improved [and] but the operation power is increased as well. The increase of the power consumption gives rise to disadvantages of degrading the circuit performance and bringing about an erroneous operation. The heat caused by the increase of the power consumption has the adverse effect on the mount of the semiconductor integrated circuit device, which disadvantageously leads to enhancing the manufacturing cost. Therefore, [the] faster operation and [the] lower power consumption have been significant issues to improving the performance of the CMOS circuit.

Page 2, paragraph beginning at line 6, has been amended as indicated below:

As a method of overcoming [the] these disadvantages, for example, reference may be [given] made to the technique disclosed in 2000 International Solid-State Circuits Conference Digest of Technical Papers, pp.294-295 (February, 2000). This technique is arranged so that a processor that is operated at high speed and low electric power may be realized by controlling the operating clock frequency and the supply voltage of a microprocessor composed of a CMOS circuit. If [the] fast operation is required, by enhancing the clock frequency and the supply voltage, the operating speed may be improved while [as] making the power consumption larger. On the other hand, if [the] slow operation is allowed, by lowering the clock frequency and the supply voltage, the power consumption may be reduced. The combinational adjustment of these controls through the operating system realizes the fast operation and the low power consumption of the microprocessor.

In the Claims:

Claims 1-16 have been cancelled without prejudice.

New claims 17-35 have been added.

FAX RECEIVED

JAN 2 8 2003

TECHNOLOGY CENTER 2800